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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P5578 Total Pages 2

First Named Inventor or Application Identifier Brian S. Doyle

Express Mail Label No. EL143562301US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 21)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 7)

4. X Oath or Declaration (Total Pages 5)

a. ___ Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ___ Computer Readable Copy
b. ___ Paper Copy (identical to computer copy)
c. ___ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))

9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_X_ b. Power of Attorney

10. _____ English Translation Document (if applicable)

11. _X_ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment

13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)

14. _____ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. _X_ Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

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18. **Correspondence Address**

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UNITED STATES PATENT APPLICATION

for

A TRANSISTOR WITH REDUCED SERIES RESISTANCE JUNCTION REGIONS

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A TRANSISTOR WITH REDUCED SERIES RESISTANCE JUNCTION REGIONS

BACKGROUND OF THE INVENTION

1). Field of the Invention

The present invention relates to a method of forming a metal-oxide-semiconductor (MOS) transistor, and to a MOS transistor.

2). Discussion of Related Art

Electronic circuits are often manufactured in and on semiconductor wafers such as silicon wafers. An electronic circuit of this kind consists of an integrated circuit of electronic components such as transistors, diodes, capacitors and other devices. One such a device which is very frequently used is a metal-oxide-semiconductor (MOS) transistor. In a MOS transistor a voltage is applied between source and drain regions and the transistor is "switched" by applying another voltage to a gate thereof. Ideally, a transistor should have a reaction time which is as fast as possible and a threshold voltage which is not exceedingly high. Figures 1a to 1e illustrate a conventional method of fabricating a conventional MOS transistor.

First, as illustrated in Figure 1a, a gate 110 is formed on a P-doped substrate 112. N-doped source and drain regions 114 are then partially formed in the substrate 112 in an ion implantation process with the gate 110

providing alignment for purposes of forming the source and drain regions 114.

Non-conductive spacers 116 are then formed next to the gate 110, as illustrated in Figure 1b. In another ion implantation process, the source and drain regions 114 are further formed with the spacers 116 providing alignment for purposes of forming the source and drain regions 114.

Next, as illustrated in Figure 1c, a metal layer 118 is deposited over the gate 110, the spacers 116, and the source and drain regions 114.

The metal layer 118 is then heated. Heating of the metal layer 118 results in a reaction between the material of the source and drain regions 114 and the metal layer 118 so that highly conductive silicide regions 120 are formed on the source and drain regions 114, as illustrated in Figure 1d. A portion of the metal layer 118 forms a metal strap between the silicide regions 120 and the gate 110. The metal strap is then etched away to finalize the fabrication of a MOS transistor 122 as illustrated in Figure 1e.

The resulting transistor 122 has silicide regions 120 through which electrical connection to the source and drain regions 114 can be made. The source and drain regions 114 have tips 124 which are located between the silicide regions 120. The tips 124 result in a relatively high series resistance between the silicide regions 120. There is reason to believe that, by locating the silicide regions in direct contact with the P-doped material of the substrate 112 (also called Schottky junctions), a transistor can be provided wherein series resistance between the silicide regions is reduced and the reaction time of the transistor is increased.

Furthermore, in order to decrease the reaction time of the transistor 122, it may be necessary to reduce a gate length 126 of the transistor. There is,

however, a risk of outdiffusion of dopants from the source and drain regions 114. A reduction in the gate length 126 of the transistor may, due to outdiffusion of dopants, result in leaking of the transistor 122. The risk of outdiffusion may be reduced by increasing the dopant concentration in the substrate 112. An increase in the dopant concentration of the substrate 112 may, however, result in a higher threshold voltage of the transistor 122. A Schottky junction type transistor and its fabrication are described in the specification of U.S. Patent No. 4, 485, 550 to Koeneke. Although the transistor in the '550 patent does hold some distinct advantages over conventional MOS transistors, it does suffer from certain disadvantages, in particular that it has a gate dielectric layer which is very thick. The gate dielectric layer also separates silicide regions from a gate electrode by a distance which substantially reduces performance of the transistor, thus necessitating the need for doped source and drain regions.

SUMMARY OF THE INVENTION

A method of forming a transistor is provided. An alignment component is formed on a substrate of a semiconductor material. A metal layer is deposited over the substrate and the alignment component. The metal layer is reacted with the semiconductor material of the substrate to form two silicide regions on opposing sides of the alignment component. The silicide regions substantially extend up to the alignment component. The alignment component is then replaced with a gate which substantially extends up to the silicide regions.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is further described by way of example with reference to the accompanying drawings wherein:

Figure 1a is a side view illustrating a substrate with a transistor gate formed thereon and source and drain regions which are partially formed after a first ion implantation step;

Figure 1b is a view similar to Figure 1a after spacers are formed next to the gate, and the source and drain regions are further formed in another ion implantation step;

Figure 1c is a view similar to Figure 1b after a metal layer is deposited;

Figure 1d is a view similar to Figure 1c after the metal layer is reacted with the substrate;

Figure 1e is a view similar to Figure 1d after a conventional MOS transistor is finally formed;

Figure 2a is a side view of a substrate with an alignment component formed thereon;

Figure 2b is a view similar to Figure 2a after a metal layer is deposited;

Figure 2c is a view similar to Figure 2b after the metal layer is reacted with the substance to form silicide regions extending up to the alignment component.

Figure 2d is a view similar to Figure 2c after an unreacted portion of the metal layer is removed;

Figure 2e is a view similar to Figure 2d after a layer is deposited;

Figure 2f is a view similar to Figure 2e after the layer is planarized to expose the alignment component;

Figure 2g is a view similar to Figure 2f after the alignment component is removed to leave an opening;

Figure 2h is a view similar to Figure 2g after a gate dielectric layer is deposited;

Figure 2i is a view similar to Figure 2h after a metal layer is deposited;

Figure 2j is a view similar to Figure 2i after the metal layer and the gate dielectric layer are planarized;

Figure 2k is a view similar to Figure 2j after the layer is removed;

Figure 3a is a view similar to Figure 2a after a dopant implantation step; and

Figure 3b is a view similar to Figure 2k with additional, doped regions.

DETAILED DESCRIPTION OF THE INVENTION

A method of forming a transistor, and the transistor are described. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be evident, however, to one skilled in the art, that the present invention may be practiced without these specific details.

An alignment component is formed on a substrate of a semiconductor material which is N- or P-doped. A metal layer is deposited over the substrate and the alignment component. The metal layer is reacted with the semiconductor material of the substrate to form two silicide regions, on opposing sides of the alignment component, which extend up to the alignment component. The alignment component is then replaced with a gate which extends up to the silicide regions. A transistor results wherein inner surfaces of the silicide regions, facing one another, are in direct contact with the N- or P-doped semiconductor material of the substrate and therefore have a low series resistance between them. There is also no need for forming source and drain regions of opposite doping of the substrate which may outdiffuse and cause leaking of the transistor. By doing away with the risk of outdiffusion and leaking of the transistor, (a) a gate length of the transistor can be reduced and (b) there is a reduced need for increasing dopant concentration within the semiconductor material of the substrate which would result in a higher threshold voltage of the transistor.

Figure 2a of the accompanying drawings illustrates a first step in forming a transistor according to the invention. A substrate 210 of a semiconductor material such as silicon is provided. The semiconductor

material is typically N or P doped. An alignment component 212 is formed on the substrate 210. The alignment component 212 may be made of a non-conductive material such as a silicon oxide or silicon nitride. The alignment component 212 may be formed according to conventional methods wherein a layer is deposited on the substrate 210, and the layer is patterned utilizing conventional photolithographic or other techniques. The alignment component may have a thickness of between 1000 Å and 2500 Å, typically in the region of about 1500 Å, and preferably has a width 214 of less than 0.10 microns although the width 214 may be less than 0.05 microns.

Next, as illustrated in Figure 2b, a metal layer 216 is deposited onto the substrate 210 and onto the alignment component 212. The metal layer 216 may be conformally deposited. The metal layer 216 may be between 300 Å and 400 Å thick, typically in the region of about 350 Å thick. The metal layer may be made of tungsten, cobalt, titanium, or any other metal forming a silicide.

Next, as illustrated in Figure 2c, the metal layer 216 is reacted with the semiconductor material of the substrate 210, typically by heating the metal layer 216 to a temperature in the region of about 700°C. Heating of the metal layer 216 results in the formation of two silicide regions 218 on opposing sides of the alignment component 212. The alignment component 212 may be made of a material which does not react with the metal layer 216 when the metal layer 216 is reacted with the semiconductor material of the substrate 210, so that a portion 220 of the metal layer 216 may remain unreacted over the alignment component 212. The silicide regions 218 have lower surfaces 222 which are located lower than a lower surface 224 of the alignment component 212. The silicide regions 218 also have inner surfaces 226, facing one another, an upper portion of which contacting the alignment component

212 and a lower portion of which contact the N- or P- doped semiconductor material of the substrate 210. A silicide region which is in contact with a semiconductor material of a substrate is also known as a "Schottky junction". Although not shown in the drawings, the silicide regions 218 may also form partially below the alignment component 212. The use of a metal layer 216 of cobalt and nickel is particularly useful for diffusing into the silicon and for forming partially below the alignment component 212.

Next, as illustrated in Figure 2d, the unreacted metal portion 220 is removed with an etchant which removes the material of the metal layer 216 selectively over the material of the alignment component 212 and the material of the silicide regions 218.

Figures 2e to 2k illustrate a method of replacing the alignment component 212 with a gate for the transistor.

First, as illustrated in Figure 2e, a layer 230 is deposited over the silicide regions 218 and the alignment component 212. The layer 230 and the alignment component 212 are made of different materials. The alignment component 212 may, for example, be made of a silicon oxide and the layer 230 may be made of silicon nitride, or vice versa. Of importance is that the material of the alignment component 212 can be selectively etched over the material of the layer 230.

Next, as illustrated in Figure 2f, the layer 230 is planarized, typically in a conventional chemical-mechanical polishing operation. Planarization is continued at least until the alignment component 212 is exposed, but without removing the layer 230 above the silicide regions 218.

Next, as illustrated in Figure 2g, the alignment component 212 is etched away utilizing an etchant which removes the material of the

alignment component 212 selectively over the material of the substrate 210, the material of the silicide regions 218, and the material of the layer 230. Removal of the alignment component 212 leaves an opening 232. The opening 232 has a lower surface 234 on the substrate 210, and side walls 236. Lower portions of the side walls 236 are defined by the upper portions of the inner surfaces 226 of the silicide regions 218 and upper portions of the side walls 236 are defined by the layer 230. The silicide regions 218 therefore extend up to the opening 232.

Next, as illustrated in Figure 2h, a gate dielectric layer 240 is deposited. The gate dielectric layer 240 forms on the layer 230, on the side walls 236 of the opening 232, and on the lower surface 234 of the opening 232. The gate dielectric layer 240 may be made of a material such as a silicon oxide (SiO_2), which has a dielectric constant of about 4, or silicon nitride (Si_3N_4) which has a dielectric constant of between about 8 and 9. The gate dielectric layer 240 may alternatively be of a material having a higher dielectric constant (a high dielectric constant material) of at least 100. A high dielectric constant material may, for example, be strontium titanate ($SrTi0_3$), barium strontium titanate (BST) or a similar mixed oxide material. The gate dielectric layer 240 is supported by the side walls 236 of the opening, allowing for the gate dielectric layer to be made relatively thin typically having a thickness of less than 100 Å. The gate dielectric layer 240 is preferably less than 10 Å in thickness if it is made of silicon dioxide. In another embodiment the gate dielectric layer 240 may, alternatively, be grown in a conventional process.

Figures 2i to 2k now illustrate how a gate electrode is formed on the gate dielectric layer 240.

First, as illustrated in Figure 2i, a metal layer 242 is deposited which covers the gate dielectric layer and fills the opening 232. The metal layer 242 may be a tungsten layer or a molybdenum layer in the case where the gate dielectric layer 242 is made of silicon dioxide or silicon nitride. Although a metal layer 242 is used as an example, it should be understood that a silicon or other semiconductor material may alternatively be used and later be doped to make it conductive. However, in the case where a high dielectric constant material is used as the gate dielectric layer 240, the metal layer 242 may be platinum or a conductive metal oxide such as ruthenium oxide (RuO_2) which will not, or will only minimally, react with the high dielectric constant material at a high temperature step.

Next, as illustrated in Figure 2j, the metal layer 242 is planarized, typically in a conventional chemical-mechanical polishing operation. Planarization is continued until the layer 230 is exposed. Once planarization is completed, a portion of the metal layer 242 remains within the opening 232, forming a gate electrode 244 of metal.

Next, as illustrated in Figure 2k, the layer 230 is removed with an etchant which removes the material of the layer 230 selectively over the material of the gate electrode 244, the material of the gate dielectric layer 240, and the material of the silicide regions 218. A metal-oxide-semiconductor (MOS) transistor 250 is so provided having a substrate 210 of semiconductor material, a gate 252 on the substrate 210, and silicide regions 218 on opposing sides of the gate 252. In an alternative method, terminal openings may be formed through the layer 230 and terminals may extend through the terminal openings and make contact with the silicide regions 218.

The gate 252 has a gate dielectric layer 240 on the substrate 210 and extending upwardly from the substrate 210 to form a surrounding spacer wall 254, and a gate electrode 244 on the gate dielectric layer 240 and within the surrounding spacer wall 254. It can be seen from the aforegoing description that the gate 252 has a gate length 214 which is determined by, and is exactly the same, as the width 214 of the alignment component 212 (see Figure 2a).

The silicide regions 218 extend up to the gate 252. The silicide regions 218 have lower surfaces 222 located lower than a lower surface 224 of the gate 252. Inner surfaces 226 of the silicide regions 218 face one another and are in direct contact with the N- or P-doped semiconductor material of the substrate 210, thus forming Schottky junctions. Because the surrounding wall 254 may be less than 10 Å thick, the gate electrode 244 may be spaced from the silicide regions 218 by less than 10 Å.

In use, an electrical voltage is applied to the silicide regions 218. A voltage may be applied to the gate electrode 244 so as to cause current to flow between the two silicide regions 218, thereby causing "switching" of the transistor 250 according to conventional semiconductor physics. Because the silicide regions form Schottky junctions, a very low series resistance exists between the silicide regions 218, thus increasing the performance of the transistor 250.

Furthermore, because the gate dielectric layer 224, and therefore also the surrounding spacer wall 254, is very thin, the gate electrode 244 operates very close to the silicide regions 218. The surrounding spacer wall 254 is therefore not a substantial cause of an increased series resistance between the silicide regions 218, especially since the silicide regions 218 are partially formed below the gate 252. Although, as previously discussed, the

surrounding spacer wall 254 is preferably less than 10 Å thick, the transistor could conceivably work with a surrounding spacer wall 254 which is less than 100 Å thick.

Furthermore, it can be seen that there is no need for the formation of source and drain regions which are oppositely doped to the remainder of the substrate 210. There is therefore no risk of outdiffusion of dopants from source and drain regions which could cause the transistor 250 to leak. The lack of doped source and drain regions which could outdiffuse has a number of advantages. Firstly, there is a reduced need for increasing the dopant concentration in the remainder of the substrate 210 which would result in a higher threshold voltage of the transistor 250. There is thus a reduced need for a high dose implant below the surface 234 (the so-called punch through implant). A dopant concentration of the substrate 210 of less than 1×10^{18} atoms per cubic centimeter may therefore suffice. Secondly, the gate length 214 of the transistor 250 can be reduced with less risk of leakage of the transistor 250. A shorter gate length 214, in turn, results in a faster transistor. A gate length 214 of less than 0.10 microns, or even less than 0.05 microns, is within the scope of the invention. The transistor 250 is therefore faster and has a lower threshold voltage due to the lack of doped source and drain regions.

As mentioned, the gate electrode 244 may be spaced from the silicide regions 218 by a very small distance, and may therefore operate very closely to the conductive silicide regions 218. Figures 3a and 3b now illustrate how additional, doped regions may be formed. The doped regions are conductive and are located even closer to the gate electrode 244.

Figure 3a is a view similar to Figure 2a after a dopant implantation step. Dopant implantation processes are known in the art. N- or P-doped regions 300 are formed next to the alignment component 212. Each doped regions 300 diffuses in underneath the alignment component 212 so that a portion 302 of the doped region 300 is located under the alignment component 212.

When the transistor is finally formed as shown in Figure 3b, the portion 302 of each doped region 300 is located below the gate 252 and extends from a respective silicide region 218 past the surrounding sidewall 254 up to a location below the gate electrode 244. The gate electrode 244 thus operates very close to the conductive doped regions 300. The portions 302 of the doped regions 300 need not be much wider than the thickness of the surrounding sidewall 254, and therefore do not substantially increase the series resistance between the two silicide regions 218. The portions 302 of the doped regions 300 typically extend in underneath the gate 252 by a distance of less than 20 Å.

Thus, a method of forming a transistor, and a transistor are described. While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely illustrative and not restrictive of the current invention, and that this invention is not restricted to the specific constructions and arrangements shown and described, since modifications may occur to those ordinarily skilled in the art.

CLAIMS

What is claimed:

1. A method of forming a transistor, comprising:

forming an alignment component on a substrate of a semiconductor material;

depositing a metal layer over the substrate and the alignment component;

reacting the metal layer with the semiconductor material of the substrate to form two silicide regions substantially extending up to the alignment component on opposing sides of the alignment component; and

replacing the alignment component with a conductive gate substantially extending up to the silicide regions.

2. The method of claim 1 wherein the alignment component is non-conductive.

3. The method of claim 2 wherein the alignment component is made of a material selected from the group consisting of a silicon oxide and silicon nitride.

4. The method of claim 1 wherein the alignment component is made of a material which does not react with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

5. The method of claim 1 wherein the alignment component has a thickness of between 1000Å and 2500Å.

6. The method of claim 1 wherein the alignment component is less than 0.10 microns wide.

7. The method of claim 1 wherein the metal layer is selected from the group consisting of a material comprising tungsten, cobalt and titanium.

8. The method of claim 1 wherein the metal layer is between 300Å and 400 Å thick.

9. The method of claim 1 wherein the silicide regions have lower surfaces located lower than a lower surface of the alignment component, and inner surfaces, facing one another, which are in contact with the semiconductor material of the substrate.

10. The method of claim 1 wherein the alignment component is replaced with the gate according to a method comprising:

depositing a layer over the silicide regions and the alignment component;

planarizing the layer at least until the alignment component is exposed;

etching the alignment component to leave an opening in the first layer; and

disposing a gate within the opening.

11. The method of claim 10 wherein, after etching of the alignment component, the silicide regions extend substantially up to the opening.

12. The method of claim 10 wherein the alignment component and the layer are made of different materials, one being made of a silicon oxide and the other being made of silicon nitride.

13. The method of claim 1 wherein the gate is formed according to a method comprising:

depositing a gate dielectric layer; and

forming a gate electrode on the gate dielectric layer.

14. The method of claim 13 wherein the gate dielectric layer is less than 10Å thick.

15. The method of claim 13 wherein the gate electrode is made out of a metal.

16. The method of claim 1, further comprising:

forming doped regions which extend from the silicide regions in underneath the gate.

17. The method of claim 13 wherein the gate dielectric layer has a dielectric constant of at least 100.

18. The method of claim 13 wherein the gate dielectric layer comprises a material selected from the group consisting of strontium titanate, and barium strontium titanate.

19. The method of claim 17 wherein the gate electrode comprises a material selected from the group consisting of platinum, a conductive metal oxide, and ruthenium oxide.

20. A transistor comprising:

a substrate of a semiconductor material;

a gate on the substrate, the gate having a gate dielectric layer, on the substrate, which is less than 100 Å thick, and a gate electrode on the gate dielectric layer; and

two silicide regions on opposing sides of the gate and substantially extending up to the gate.

21. The transistor of claim 20 wherein the silicide regions have lower surfaces located lower than a lower surface of the gate, and inner surfaces, facing one another, which are in contact with the semiconductor material of the substrate wherein the substrate has the same type dopant from the one silicide region to the other silicide region.

22. The transistor of claim 20 wherein the gate has a gate length of less than 0.10 microns.

23. The transistor of claim 20 wherein the gate comprises:

a spacer wall between the gate electrode and one of the silicide regions, the spacer wall being less than 100 Å thick.

24. The transistor of claim 20 wherein a single layer forms both the gate dielectric layer and the spacer wall.

25. The transistor of claim 20, further comprising:

a respective doped region which extends from a respective silicide region in underneath the gate.

ABSTRACT OF THE DISCLOSURE

An alignment component is formed on a substrate of a semiconductor material which is N- or P-doped. A metal layer is deposited over the substrate and the alignment component. The metal layer is reacted with the semiconductor material of the substrate to form two silicide regions, on opposing sides of the alignment component, which extend up to the alignment component. The alignment component is then replaced with a gate which extends up to the silicide regions. A transistor results wherein inner surfaces of the silicide regions, facing one another, are in direct contact with the N- or P-doped semiconductor material of the substrate and therefore have a low series resistance between them.

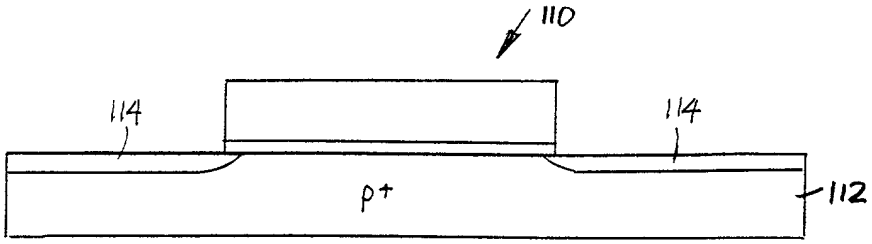

FIG 1a

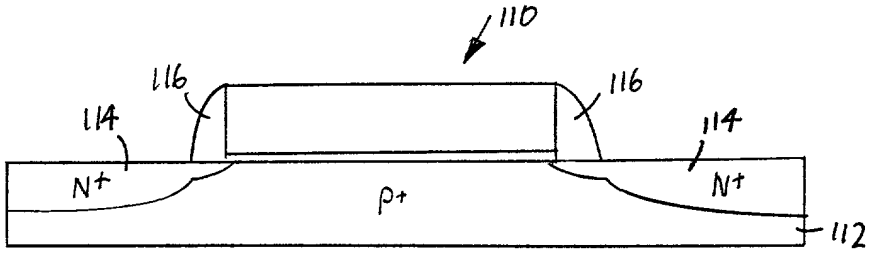

FIG 1b

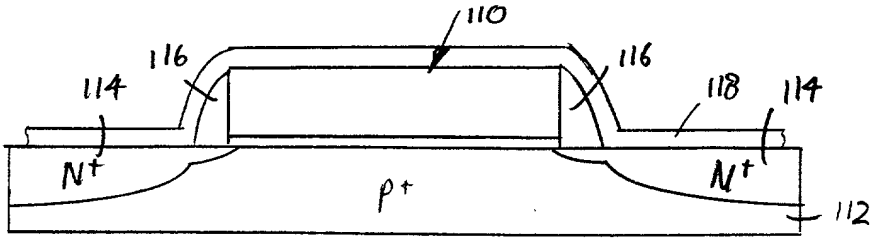

FIG 1c

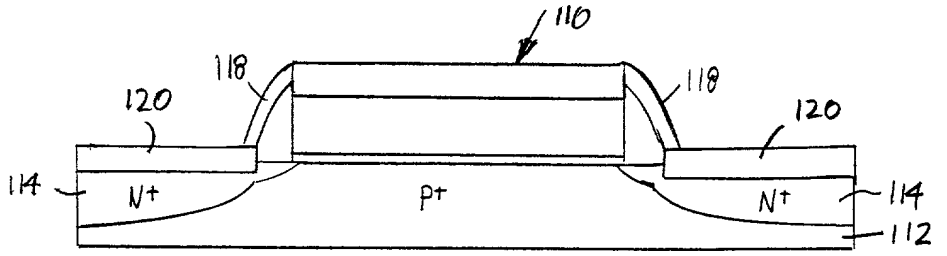

FIG 1d

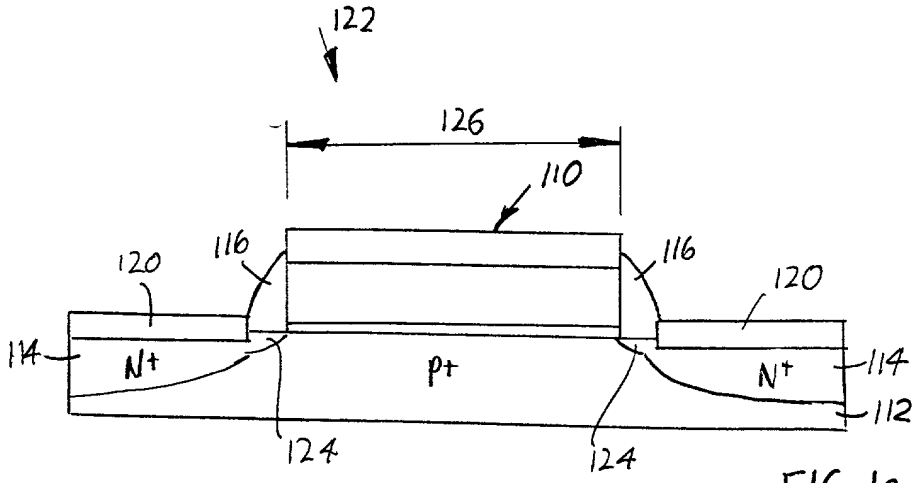

FIG 1e

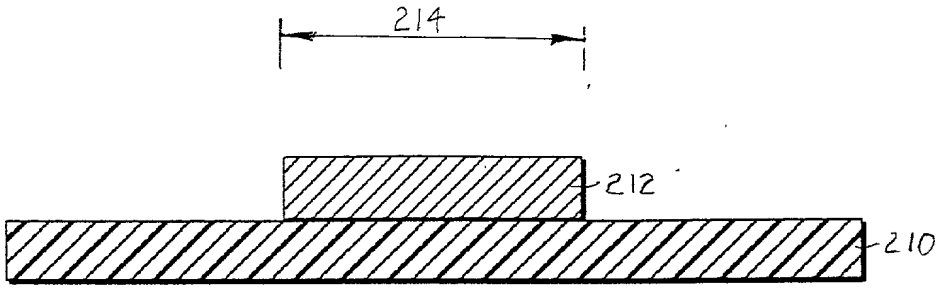

Fig. 2a

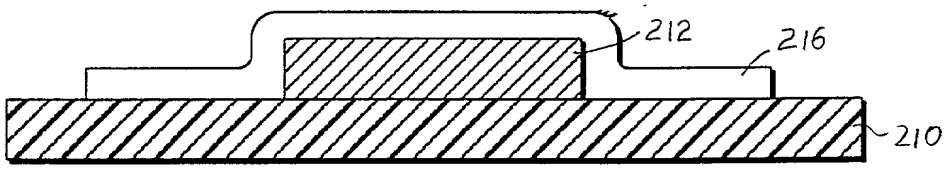

Fig. 2b

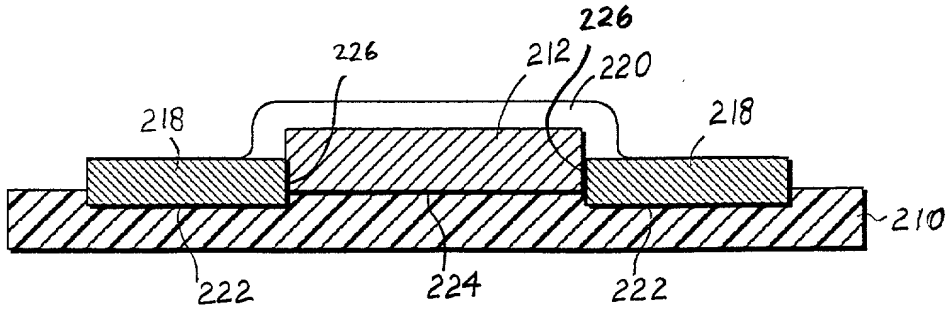

Fig. 2c

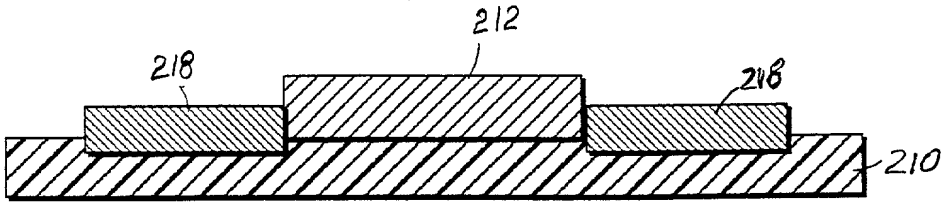

Fig. 2d

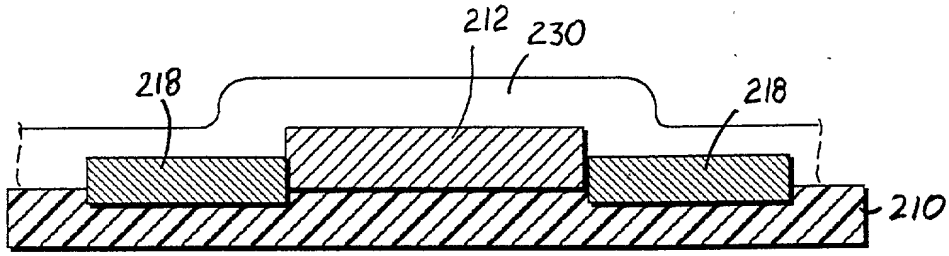

Fig. 2e

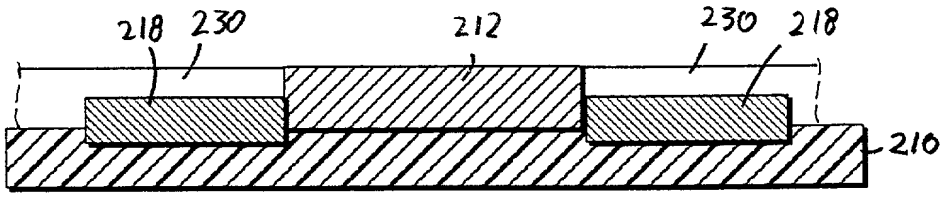

Fig. 2f

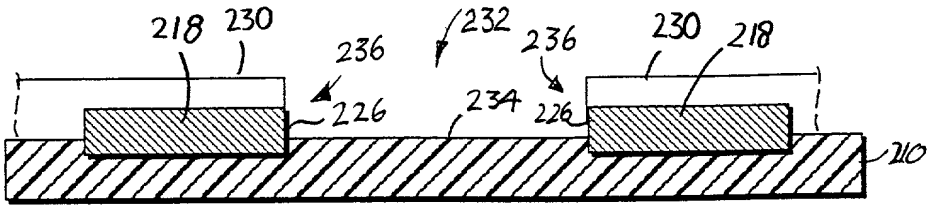

Fig. 2g

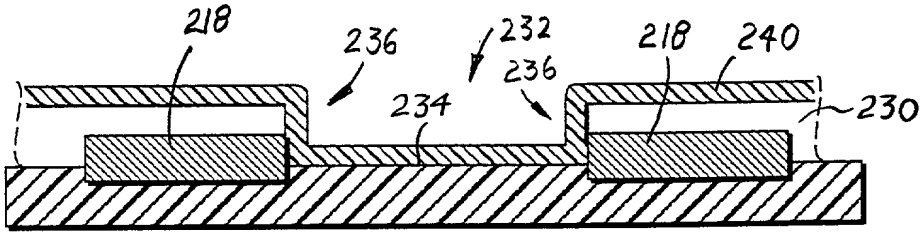

Fig. 2h

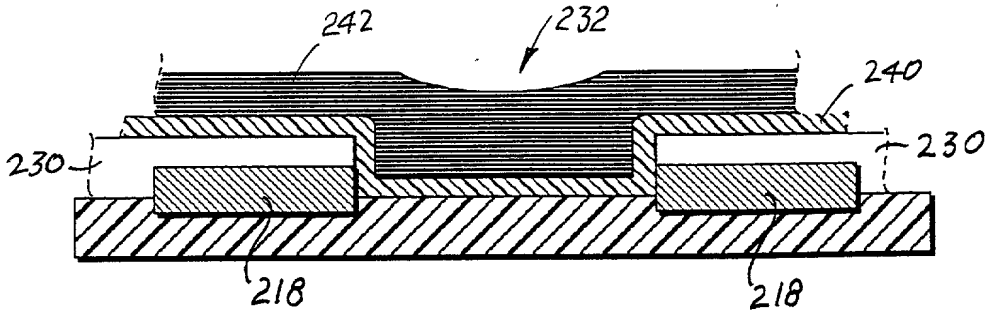

Fig. 2i

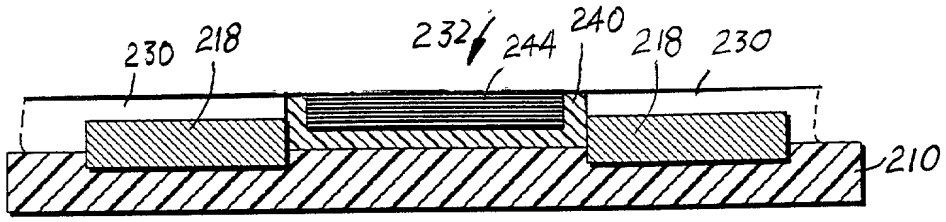
230
218
232
244
240
218
230
210

Fig. 2j

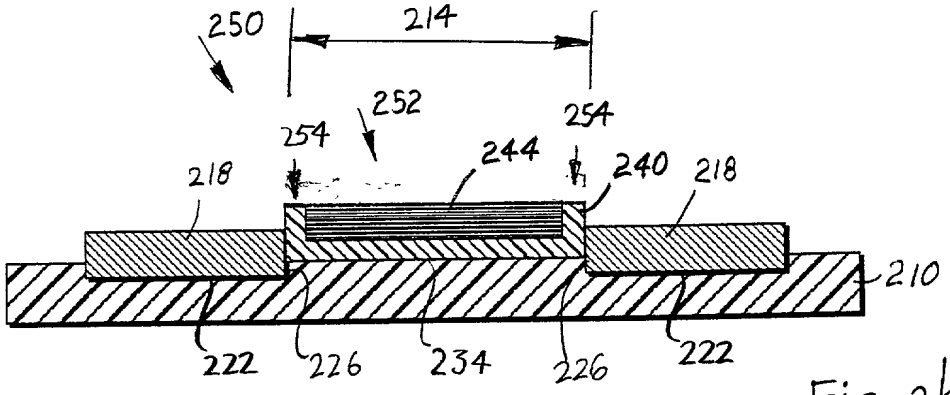
250
214
252
254
254
218
244
240
218
210
222
226
234
226
222

Fig. 2k

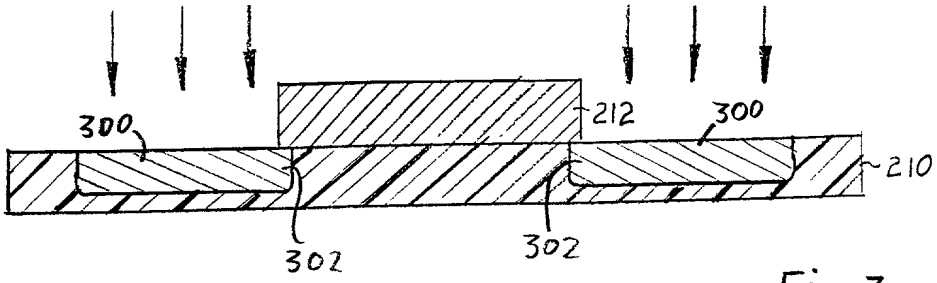
300
212
300
210
302
302

Fig. 3a

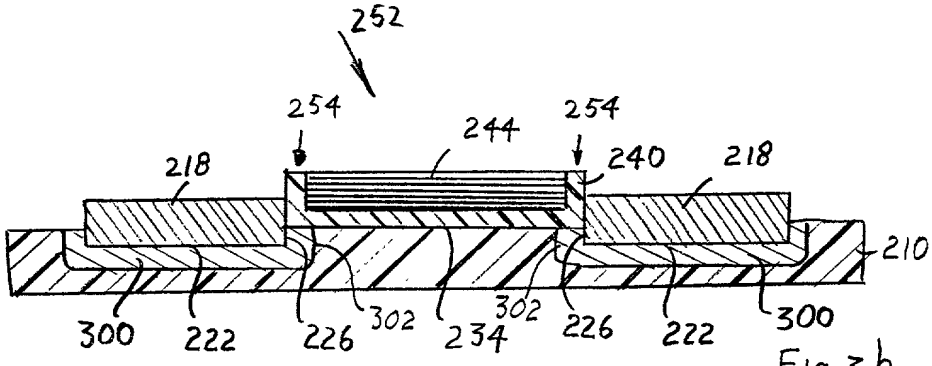
252
254
244
254
218
240
218
210
300
222
226
302
234
302
226
222
300

Fig. 3b

Attorney's Docket No.: 42390.P5578 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A TRANSISTOR WITH REDUCED SERIES RESISTANCE JUNCTION REGIONS

the specification of which

__XX__ is attached hereto.

_____ was filed on _____ as United States Application Number _____ or PCT International Application Number_____ and was amended on _____. (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor s certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below

(Application Number)	Filing Date
(Application Number)	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Number)	Filing Date	(Status -- patented, pending, abandoned)
(Application Number)	Filing Date	(Status -- patented, pending, abandoned)

I hereby appoint Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; Amy M. Armstrong, Reg. No. 42,265; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Kent M. Chen, Reg. No. 39,630; Lawrence M. Cho, Reg. No. 39,942; Yong S. Choi, Reg. No. P43,324; Thomas M. Coester, Reg. No. 39,637; Roland B. Cortes, Reg. No. 39,152; Barbara Bokanov Courtney, Reg. No. 42,442; Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; Richard Leon Gregory, Jr., Reg. No. 42,607; Dinu Gruia, Reg. No. P42,996; David R. Halvorson, Reg. No. 33,395; Thomas A. Hassing, Reg. No. 36,159; Phuong-Quan Hoang, Reg. No. 41,839; Willmore F. Holbrow III, Reg. No. P41,845; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. ß 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Thinh V. Nguyen, Reg. No. 42,034; Kimberley G. Nobles, Reg. No. 38,255; Michael A. Proksch, Reg. No. 43,021; Babak Redjaian, Reg. No. 42,096; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Anand Sethuraman, Reg. No. P43,351; Charles E. Shemwell, Reg. No. 40,171; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Allan T. Sponseller, Reg. No. 38,318; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; George G. C. Tseng, Reg. No. 41,355; Lester J. Vincent, Reg. No. 31,460; John Patrick Ward, Reg. No. 40,216; Stephen Warhola, Reg. No. 43,237; Charles T. J. Weigell, Reg. No. 43,398; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my attorneys, and James A. Henry, Reg. No. 41,064; Daniel E. Ovanezian, Reg. No. 41,236; Glenn E. Von Tersch, Reg. No. 41,364; and Chad R. Walsh, Reg. No. 43,235; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Jeffrey S. Draeger, Reg. No. 41,000; Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells, Reg. No. P43,256; and Alexander Ulysses Witkowski, Reg. No. P43,280; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Michael A. Bernadicou, BLAKELY, SOKOLOFF, TAYLOR &
(Name of Attorney or Agent)
ZAFMAN LLP, 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025 and direct telephone calls to Michael A. Bernadicou, (408) 720-8598.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the

United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature ______________________ Date ______________

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Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by ßß1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.